

ABSTRACT OF THE DISCLOSURE:

A CMOS logic circuit is disclosed wherein the number of kinds of basic parts is suppressed to five to allow designing of a circuit which operates at a high speed and repetitiveness of wiring lines is increased to allow designing of a circuit which is simple in circuit scale and high in expandability and besides the time required for adjustment of components is reduced significantly to reduce the man-hours for arrangement significantly to reduce the man-hours for development significantly and the same basic parts are used so as to achieve augmentation of the yield and promote reduction of the production cost.